Fig.1

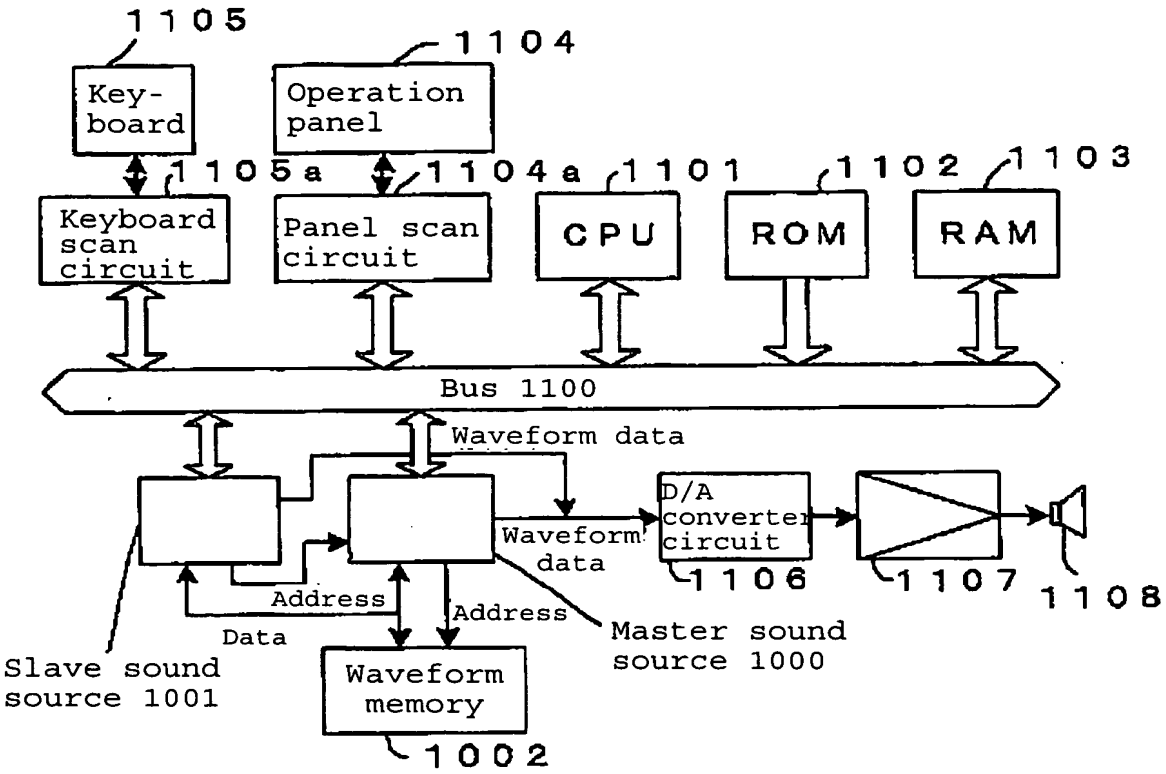

1105
1104
Key-board
Operation panel
1105a
1104a
1101
1102
1103
Keyboard scan circuit
Panel scan circuit
CPU
ROM
RAM
Bus 1100
Waveform data
D/A converter circuit
Waveform data
1106
1107
1108
Address
Data
Address
Slave sound source 1001
Master sound source 1000
Waveform memory
1002

Fig. 2

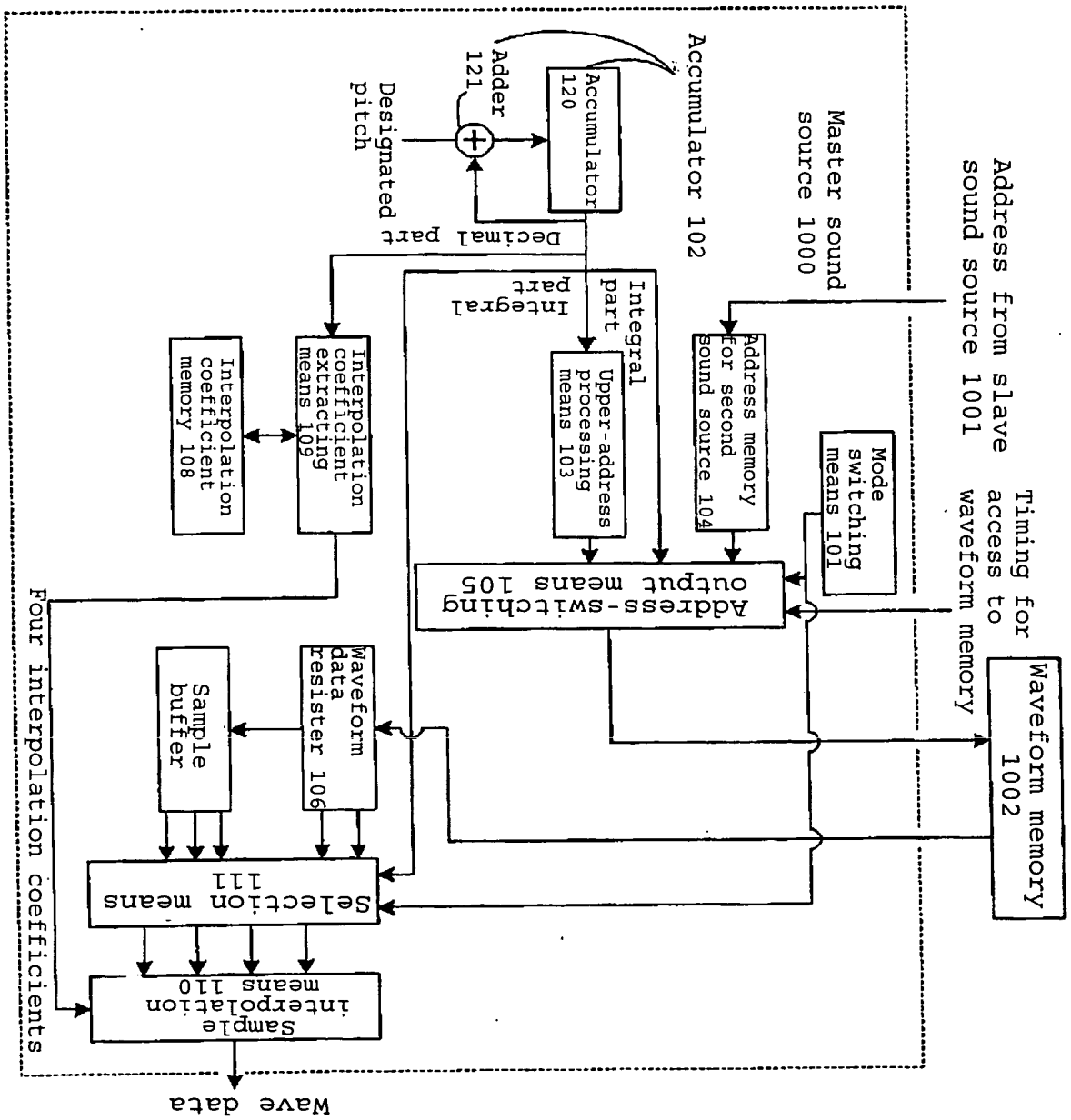

Address from slave sound source 1001
Timing for access to waveform memory
Waveform memory 1002
Master sound source 1000
Accumulator 102
Accumulator 120
Adder 121
Designated pitch
Decimal part
Integral part
Integral part
Upper-address processing means 103
Address memory for second sound source 104
Mode switching means 101
Address-switching output means 105
Interpolation coefficient extracting means 109
Interpolation coefficient memory 108
Four interpolation coefficients
Waveform data resister 106
Sample buffer
Selection means 111
Sample interpolation means 110
Wave data

Fig.3

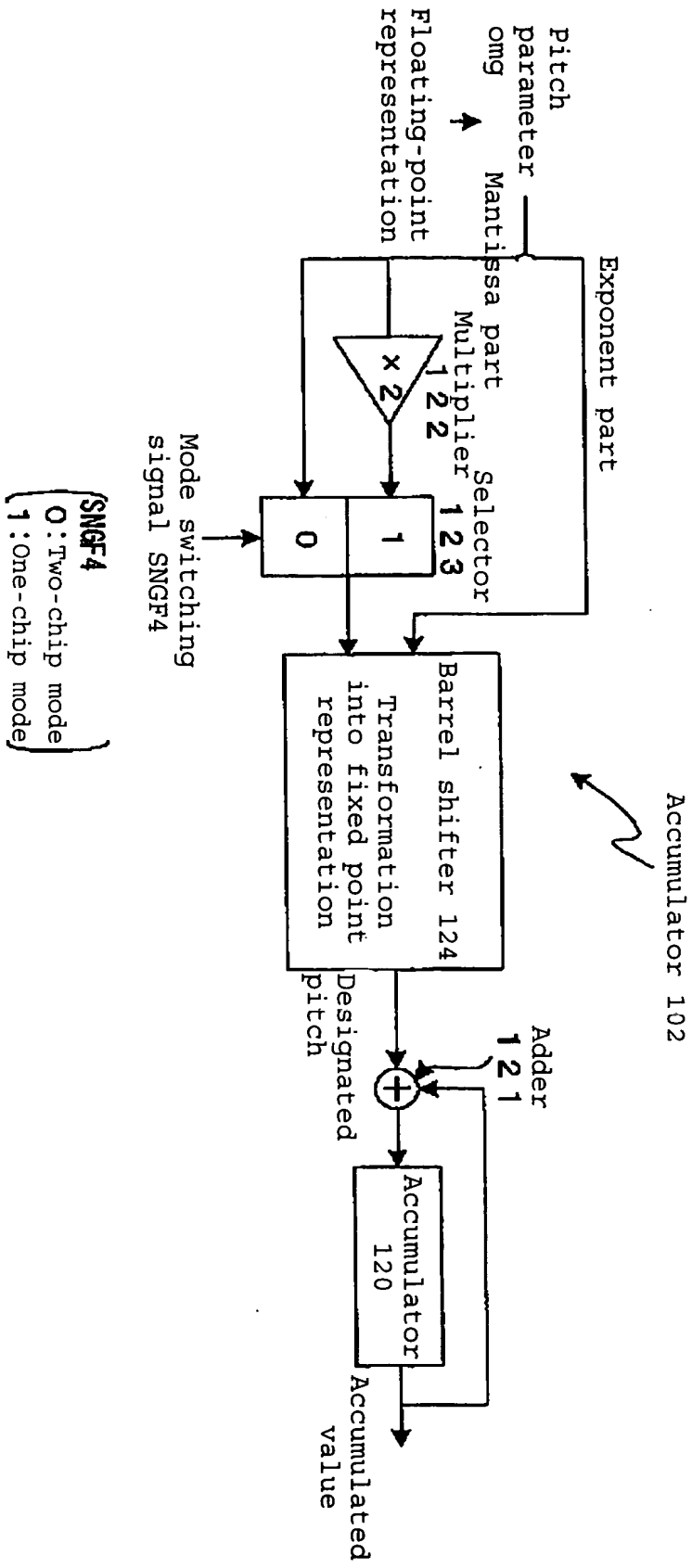

Pitch parameter omg
Floating-point representation
Mantissa part
Exponent part
Multiplier 122
× 2
Selector 123
0
1
Mode switching signal SNGF4
SNGF4
0 : Two-chip mode
1 : One-chip mode
Barrel shifter 124
Transformation into fixed point representation
Designated pitch
Adder 121
Accumulator 120
Accumulated value
Accumulator 102

Fig. 4

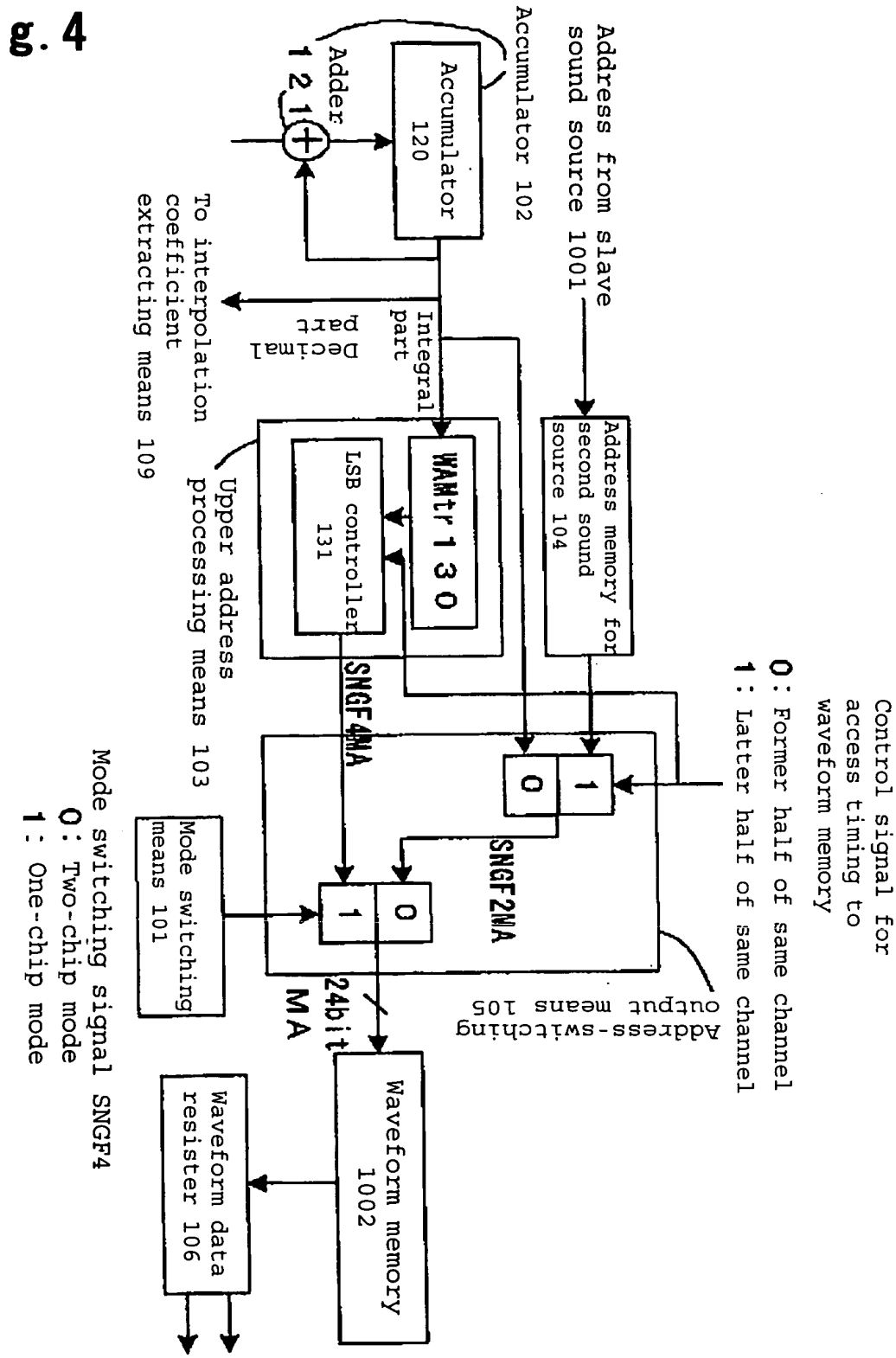

Address from slave sound source 1001
Accumulator 102
Accumulator 120
Adder 121
Integral part
Decimal Part
To interpolation coefficient extracting means 109
Upper address processing means 103
WAMtr130
LSB controller 131
Address memory for second sound source 104
SNGF4MA
SNGF2MA
Address-switching output means 105
Mode switching means 101
24bit MA
Waveform memory 1002
Waveform data resister 106
Control signal for access timing to waveform memory
0: Former half of same channel
1: Latter half of same channel
Mode switching signal SNGF4
0: Two-chip mode
1: One-chip mode

Fig. 5

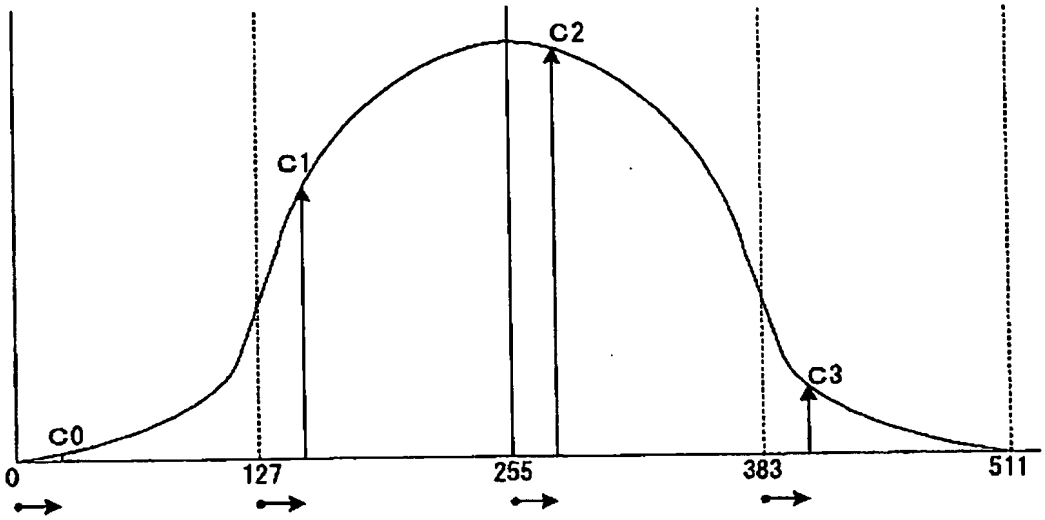
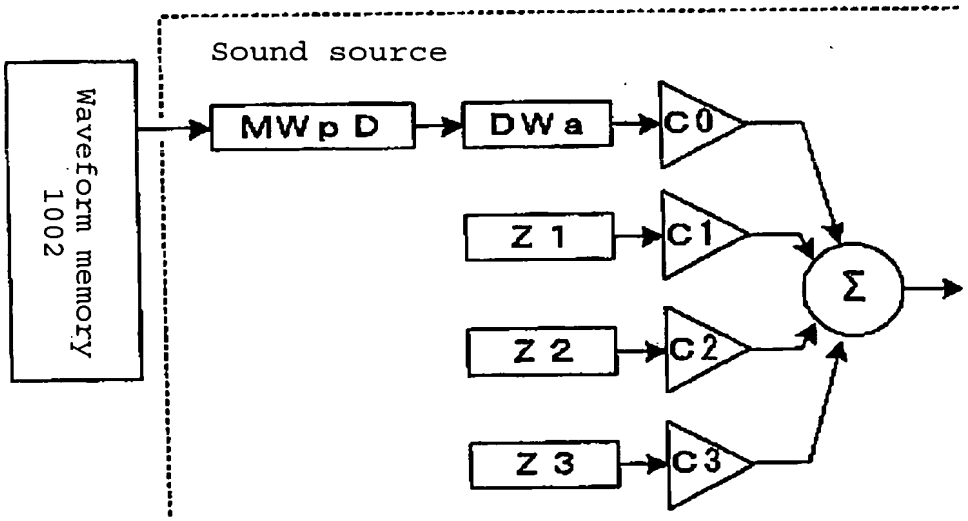
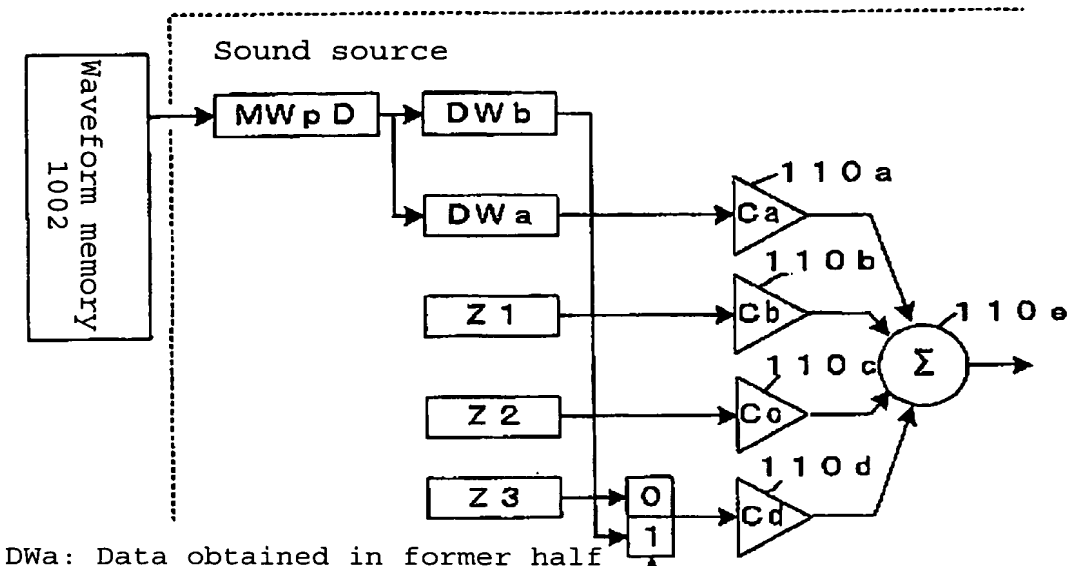



Fig. 6




Whenever one sample proceeds, data are renewed in the direction of Z3←Z2←Z1←DWa

# Fig. 7




DWa: Data obtained in former half
DWb: Data obtained in latter half

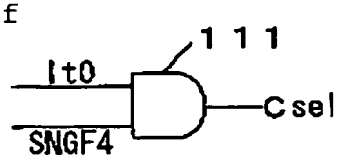
Csel

Ca=(Csel==0)? C0 : C1 :
Cb=(Csel==0)? C1 : C2 :
Cc=(Csel==0)? C2 : C3 :
Cd=(Csel==0)? C3 : C0 ;

# Fig. 8

LSB indicative of address in waveform memory

Mode switching signal




| ltO | SNGF4 | Csel |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Whenever two samples proceed, data are renewed as in the form of Z3←Z1, Z2←DWa and Z1←DWb

Fig.9

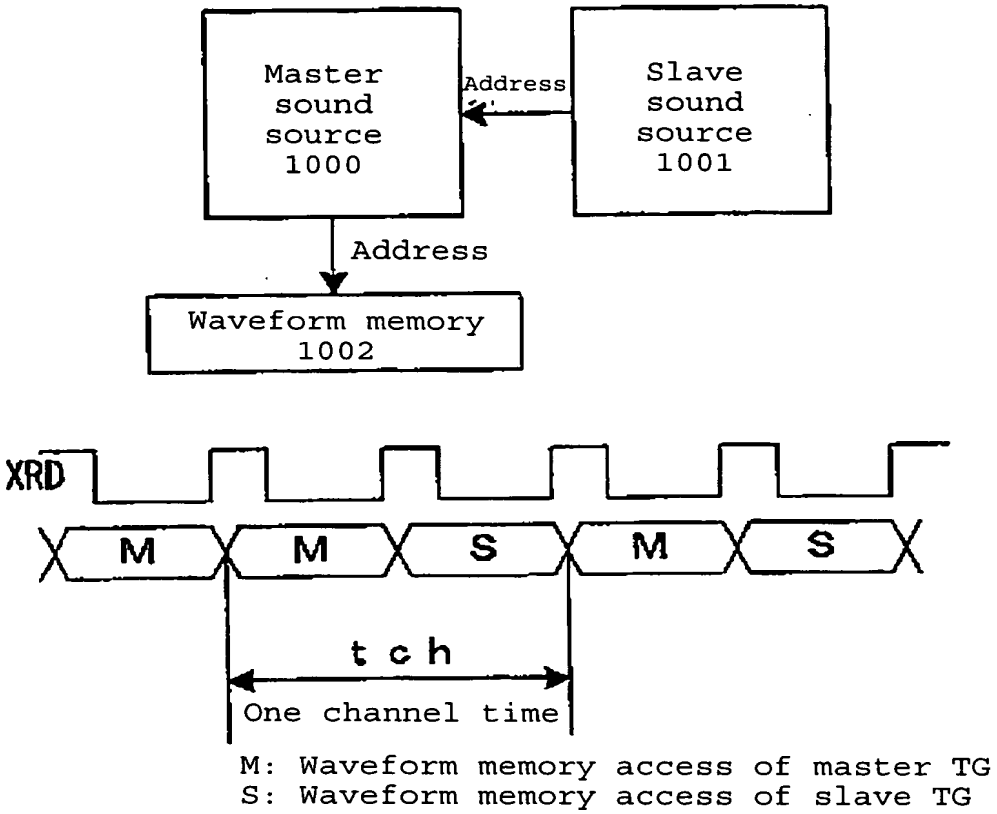
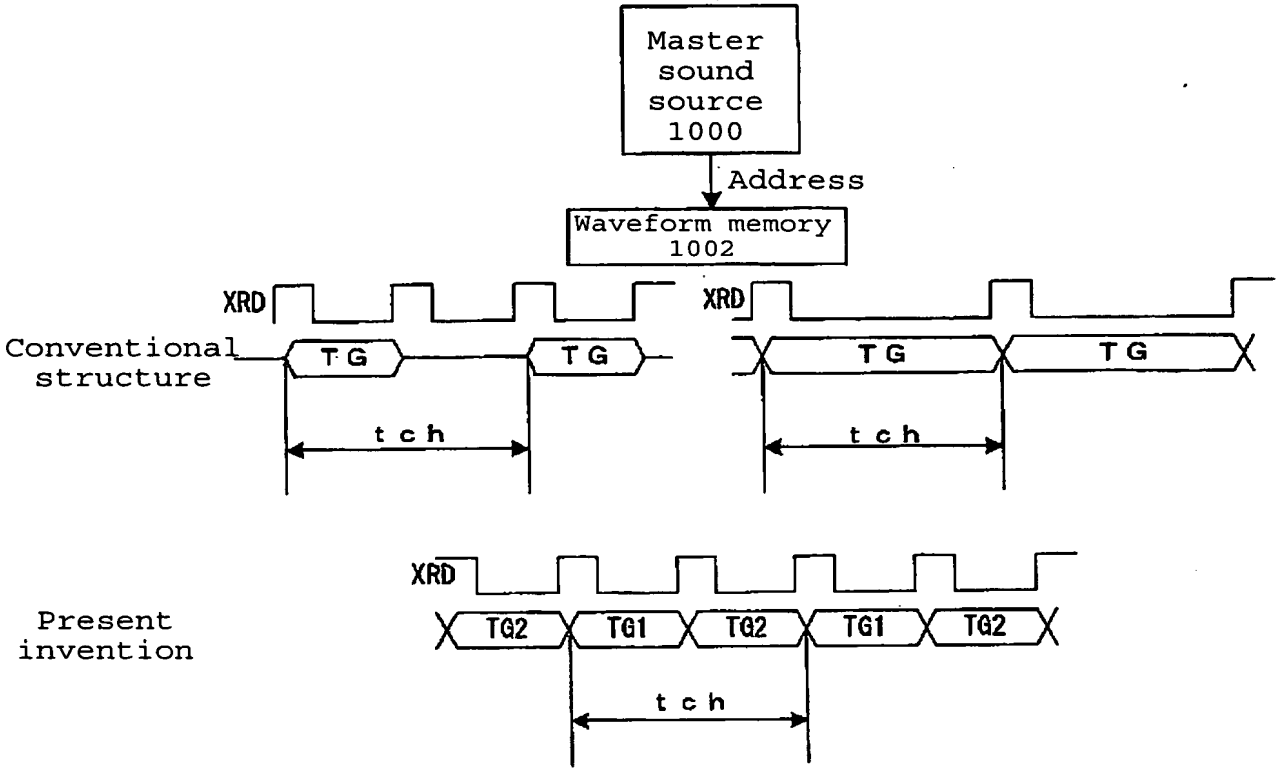

Master sound source 1000
Address
Slave sound source 1001
Address
Waveform memory 1002
XRD
M
M
S
M
S
t c h
One channel time
M: Waveform memory access of master TG
S: Waveform memory access of slave TG

Fig.10




TG1: Access in former half of same channel
TG2: Access in latter half of same channel

Fig.11

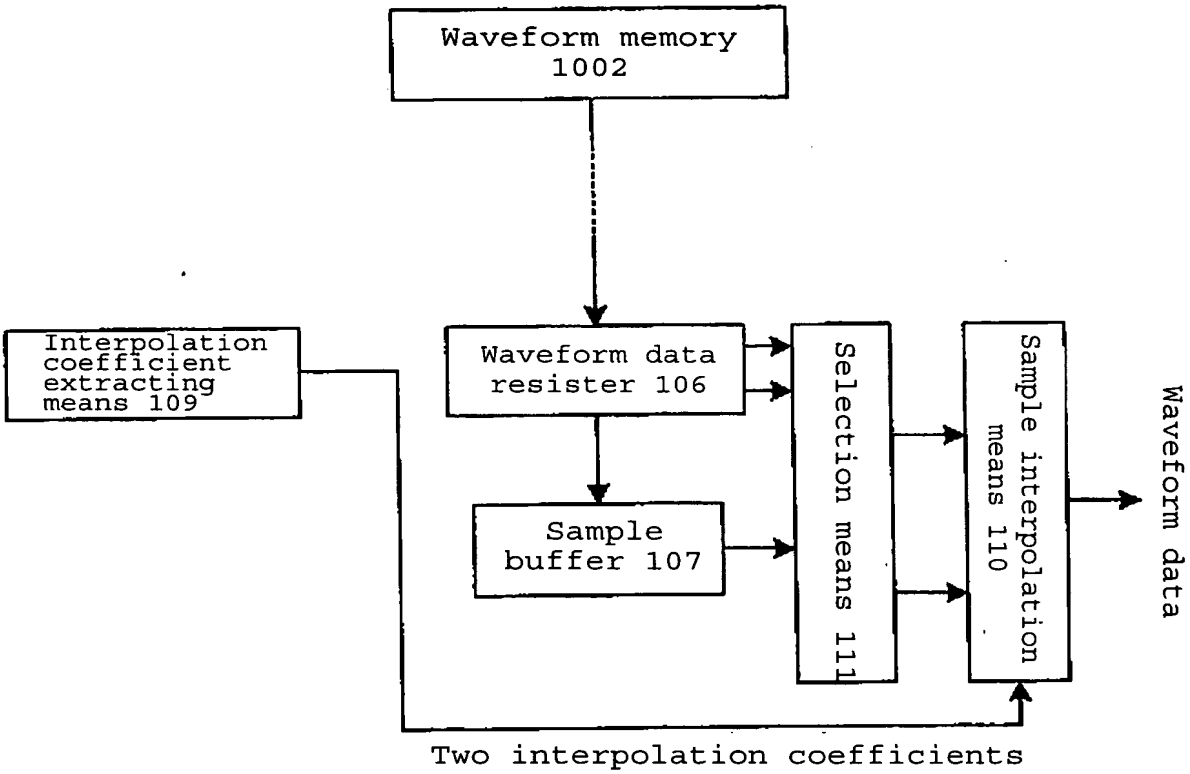

Waveform memory 1002
Interpolation coefficient extracting means 109
Waveform data resister 106
Sample buffer 107
Selection means 111
Sample interpolation means 110
Waveform data
Two interpolation coefficients

Fig.12

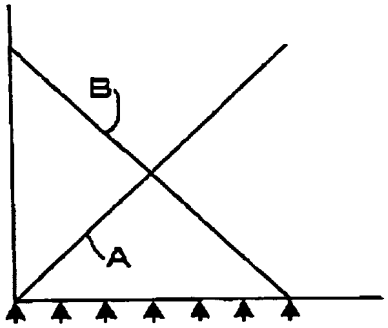

B
A

Fig.13

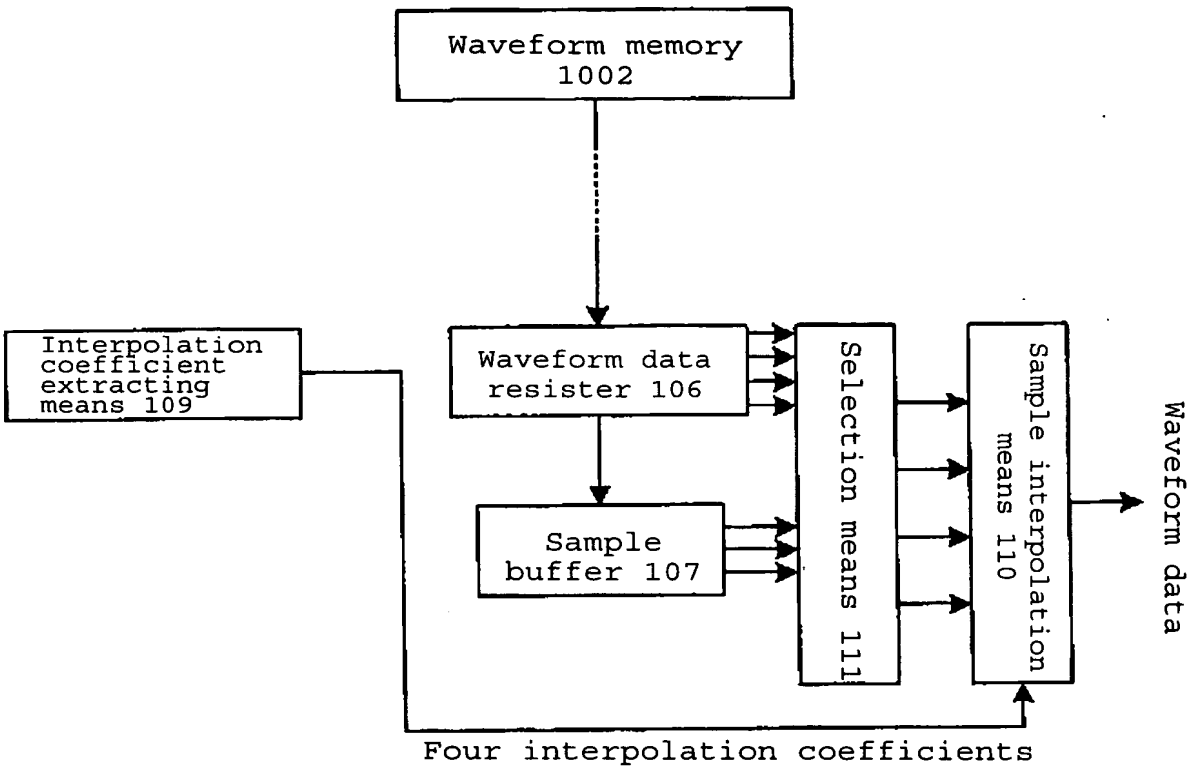

Waveform memory 1002
Interpolation coefficient extracting means 109
Waveform data resister 106
Sample buffer 107
Selection means 111
Sample interpolation means 110
Waveform data
Four interpolation coefficients

Fig.14

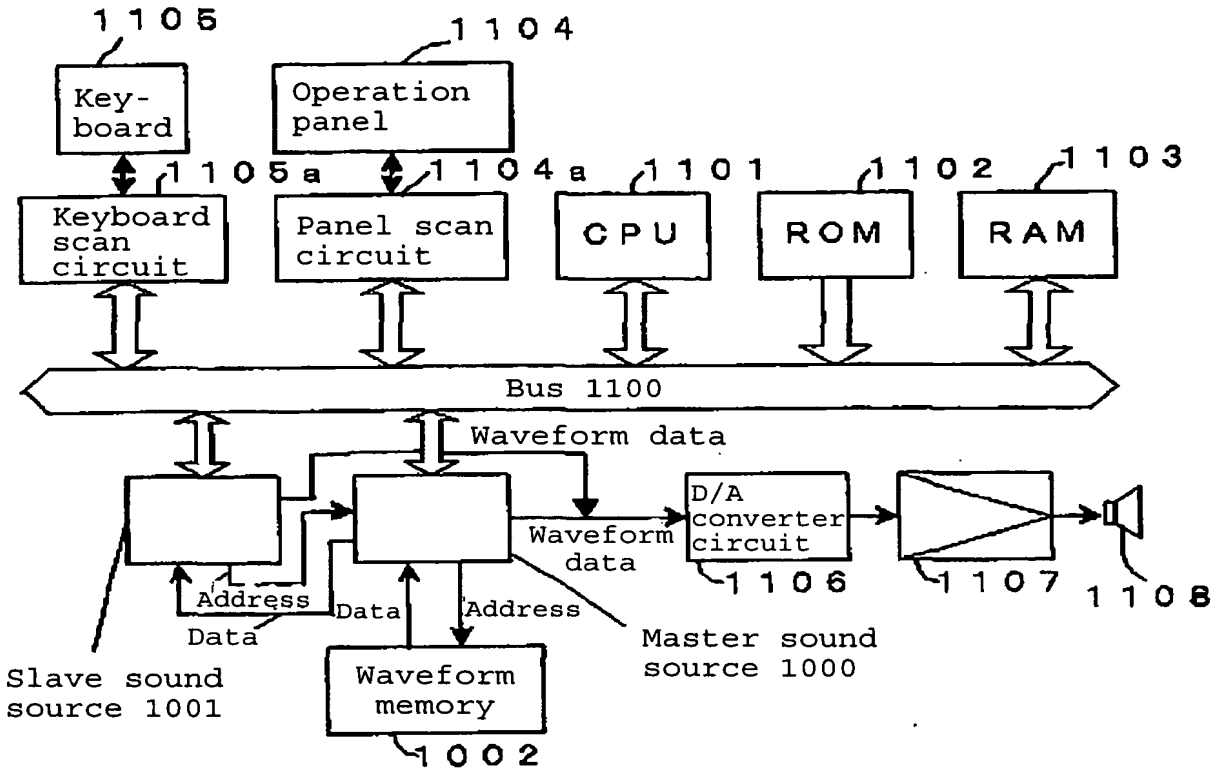

1105
Key-board
1104
Operation panel
1105a
1104a
1101
1102
1103
Keyboard scan circuit
Panel scan circuit
CPU
ROM
RAM
Bus 1100
Waveform data
D/A converter circuit
Waveform data
1106
1107
1108
Address
Data
Data
Address
Slave sound source 1001
Waveform memory
1002
Master sound source 1000

Fig. 15

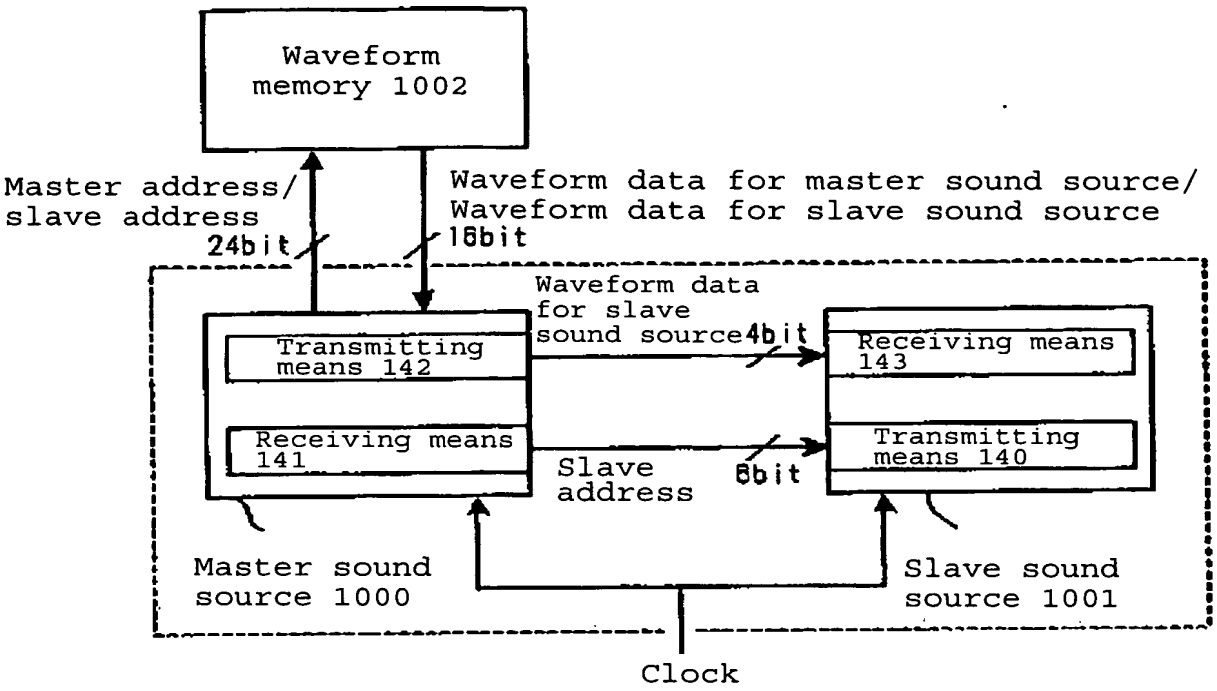

Waveform memory 1002
Master address/ slave address
24bit
Waveform data for master sound source/ Waveform data for slave sound source
16bit
Waveform data for slave sound source
4bit
Transmitting means 142
Receiving means 141
Receiving means 143
Transmitting means 140
Slave address
8bit
Master sound source 1000
Slave sound source 1001
Clock

Fig. 16

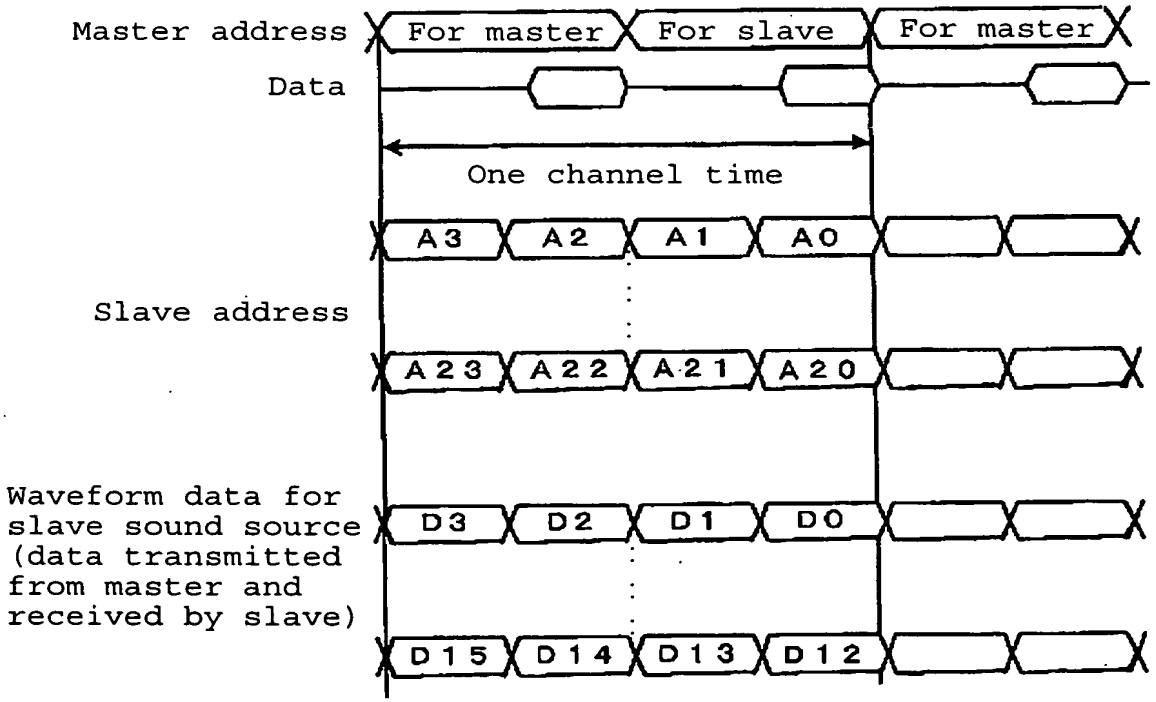

Master address
For master
For slave
For master
Data
One channel time
A3
A2
A1
A0
Slave address
A23
A22
A21
A20
Waveform data for slave sound source (data transmitted from master and received by slave)
D3
D2
D1
D0
D15
D14
D13
D12

Fig.17

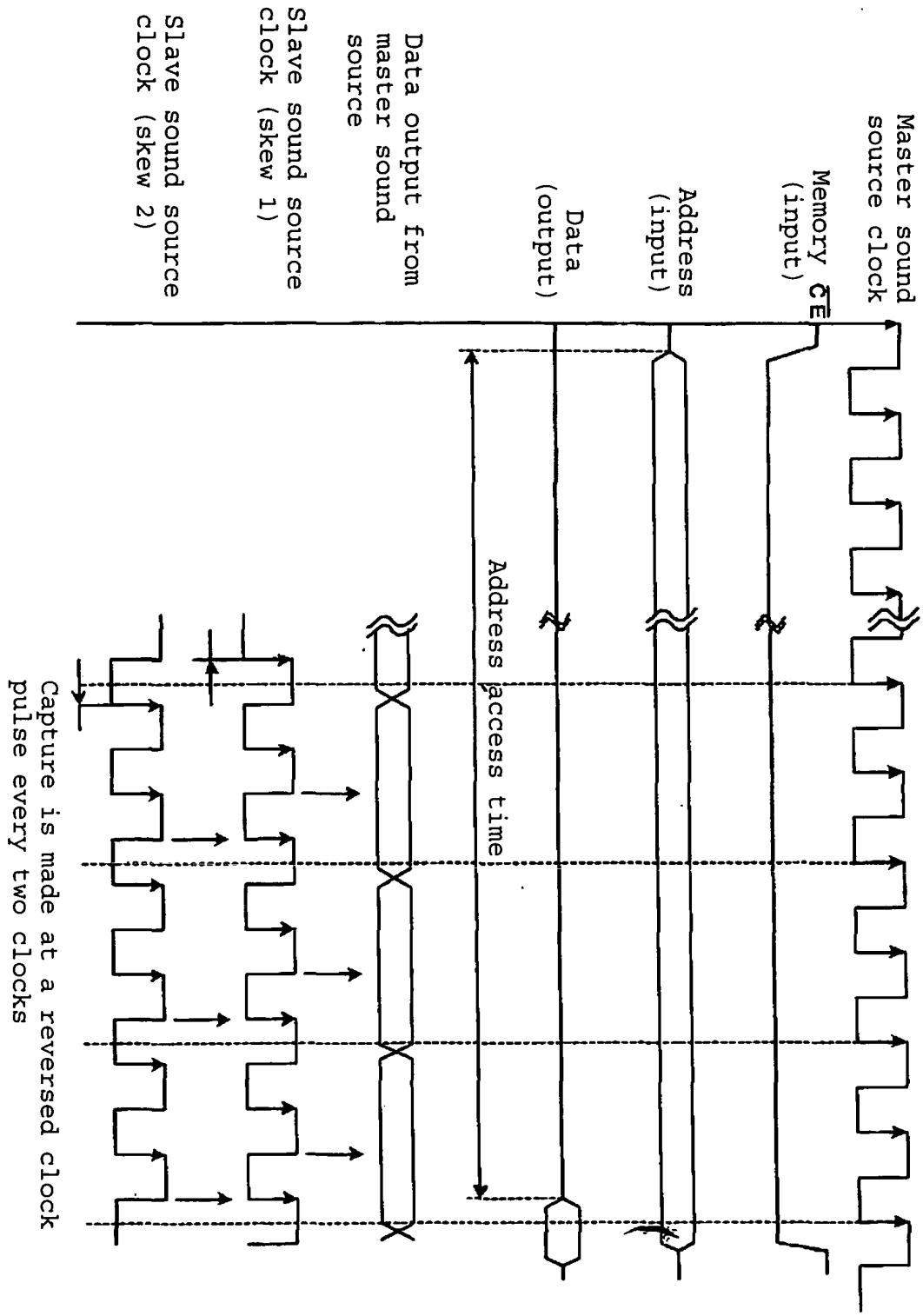
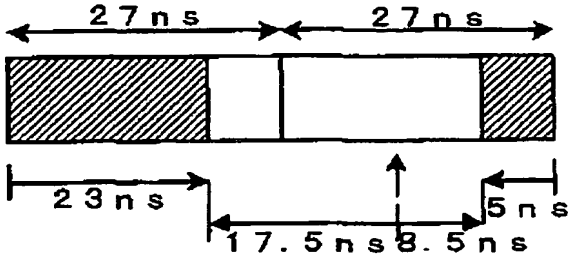

Master sound source clock
Memory CE (input)
Address (input)
Data (output)
Data output from master sound source
Slave sound source clock (skew 1)
Slave sound source clock (skew 2)
Address access time
Capture is made at a reversed clock pulse every two clocks

Fig.18



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| Functions of circuit blocks and the like | Number of output terminals | Number of input terminals |
|---|---|---|
| A: External memory access circuit | 24 | 16 |
| B: Address-output/data-input for slave sound source | 7 | 4 |
| 1105a: Keyboad scan circuit | 5 | 8 |
| 150: Data-output/address-input for master sound source | 4 | 7 |

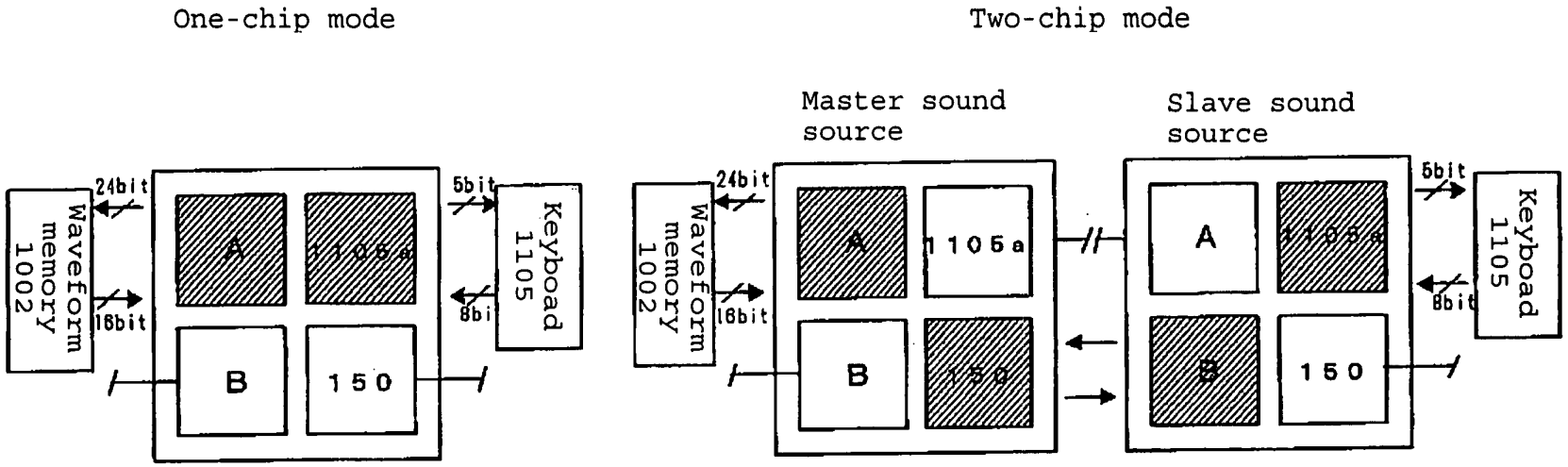



Fig.19

Fig.20

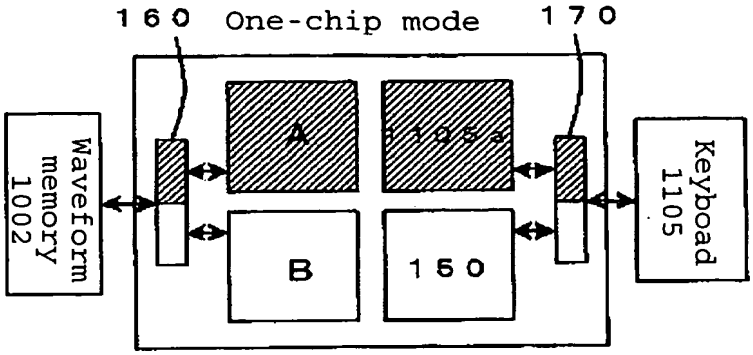



Fig.21

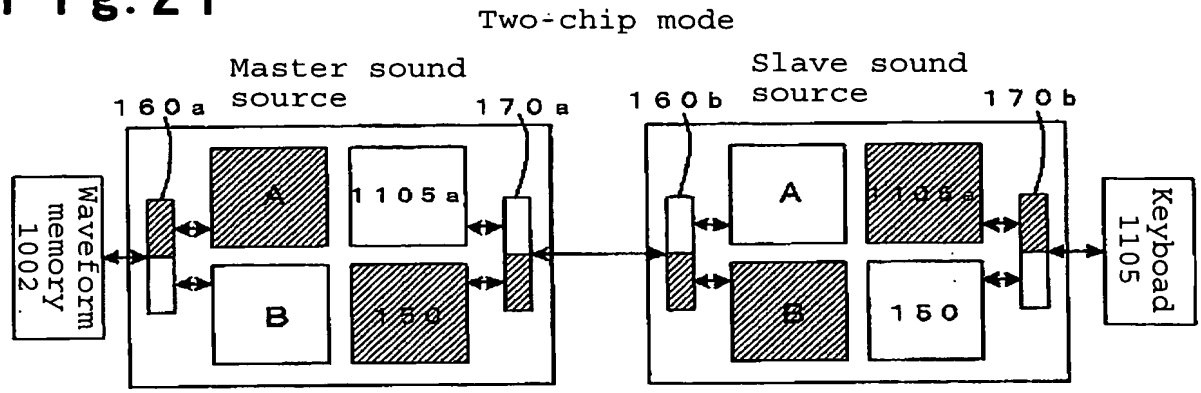



Fig.22

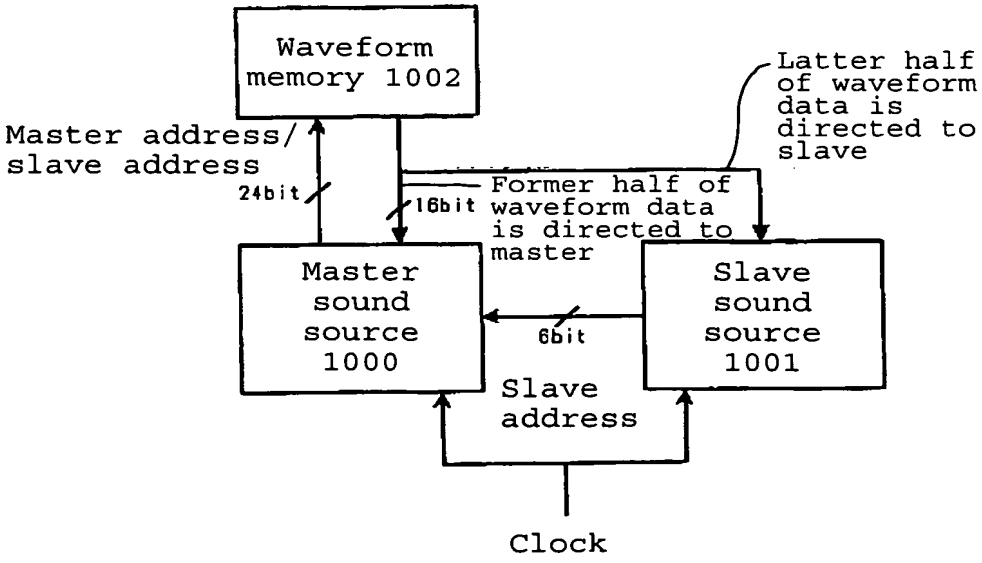


Fig.23

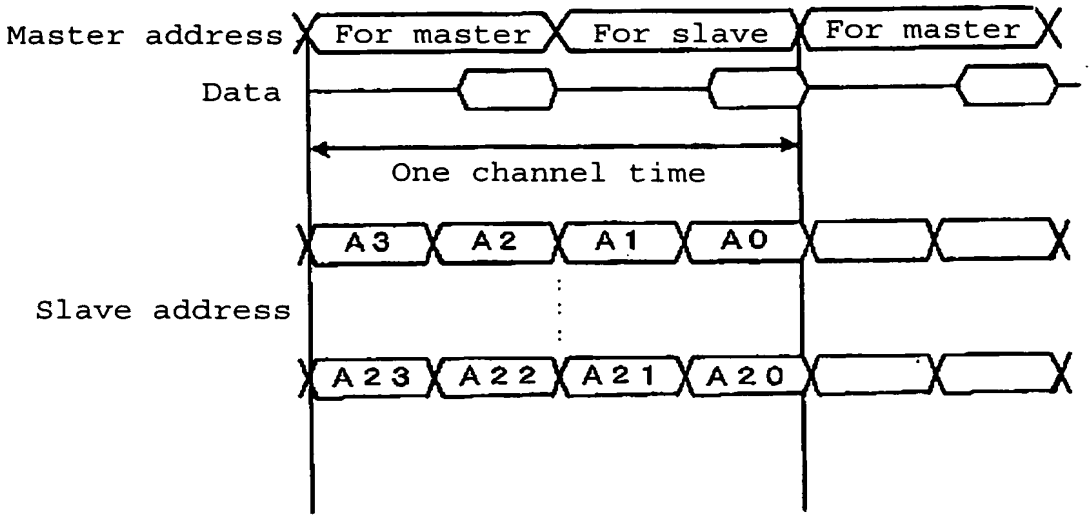



Fig.24

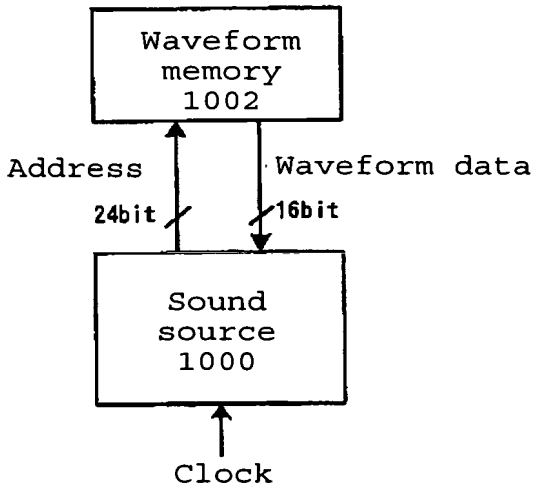



Fig.25

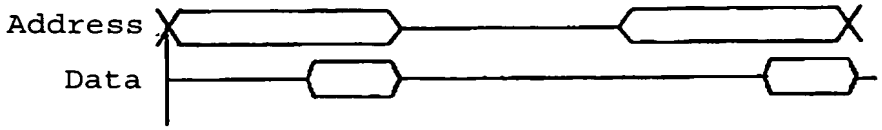
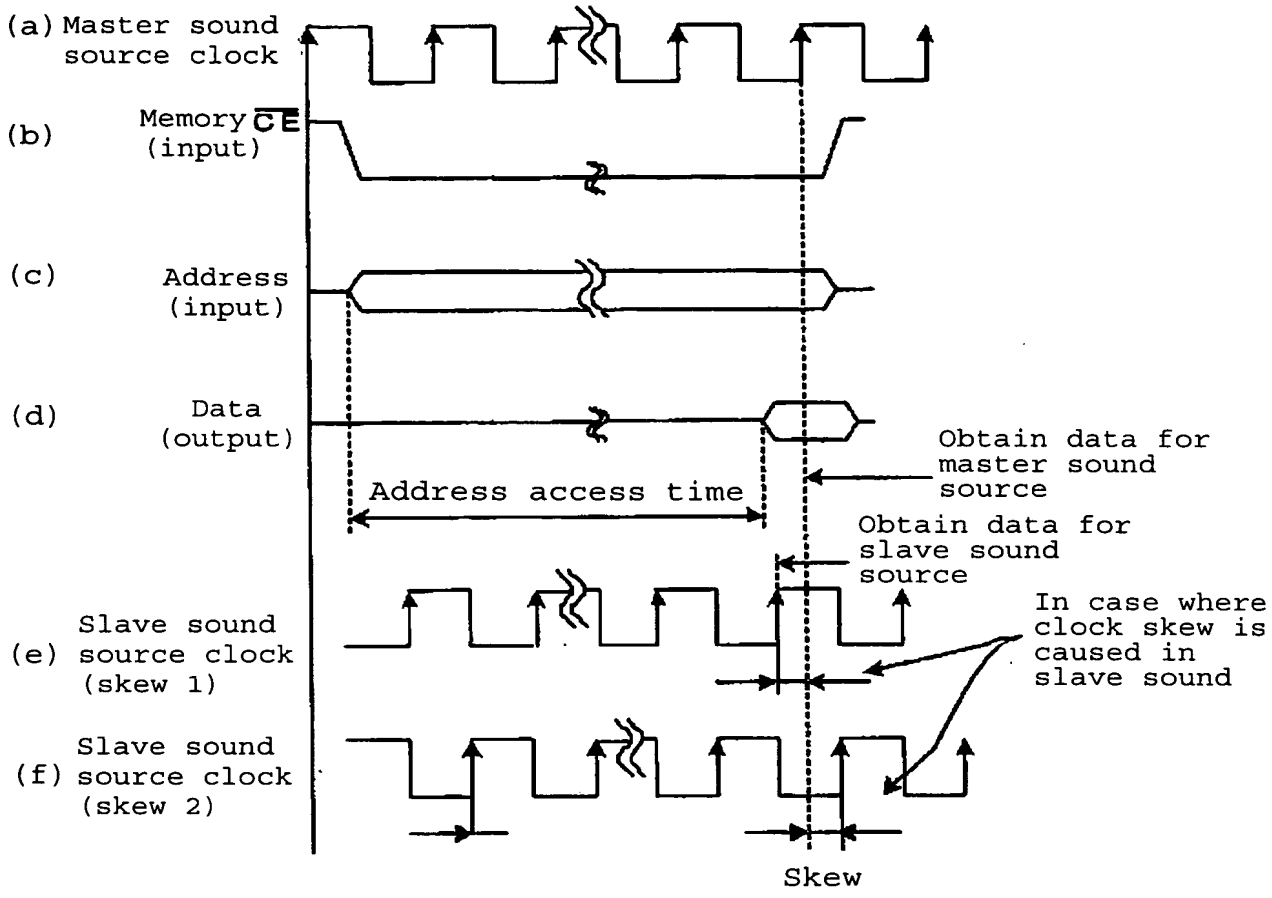


Fig. 26


(a) Master sound source clock
(b) Memory $\overline{CE}$ (input)
(c) Address (input)
(d) Data (output)
Address access time
Obtain data for master sound source
Obtain data for slave sound source
(e) Slave sound source clock (skew 1)
(f) Slave sound source clock (skew 2)
In case where clock skew is caused in slave sound
Skew